REMARKS/ARGUMENTS

The foregoing amendment and the following arguments are provided to impart precision to the claims, by more particularly pointing out the invention, rather than to avoid prior art.

Claim Objections

The Examiner objected to claims 1 and 4. Claims 1 and 4 have been amended to overcome these objections.

35 U.S.C. § 102 Rejections

Examiner rejected claims 1-3 under 35 U.S.C. § 102(e) as being anticipated by U.S. Patent No. 6,303,448 (hereinafter "Chang").

Claim 1, as amended, includes a limitation of a gate dielectric layer disposed superjacent the bottom portion of the recess, adjacent the substantially vertical sidewalls, *and superjacent a portion of a top surface of the substrate*. Chang does not teach such a limitation, and therefore does not anticipate claim 1.

As can be seen in Figures 5 and 6 of Chang, a gate oxide layer is formed in a trench (Col. 4, lines 47-51). The gate oxide layer 62 does not extend over any higher portion of the substrate 10. Moreover, as can be seen in Figures 1 and 2, the trench 50 is formed at a uniform depth. Further, since the gate oxide 62 is deposited before the barrier layer 14 is removed from the substrate 10, the top surface of the substrate 10 is never exposed when the gate oxide 62 is deposited. Therefore, the gate oxide 62 is not deposited over the top surface of the substrate 10, and claim 1 is not anticipated by Chang.

Claims 2 and 3 depend from the independent claim 1, and therefore include all the limitations of claim 1. As a result, since claim 1 is not anticipated by Chang, claims 2 and 3 are also not anticipated by Chang.

Examiner rejected claims 4-6 under 35 U.S.C. § 102(a) as being anticipated by U.S. Patent No. 5,918,134 (hereinafter "Gardner").

Claim 4 includes a limitation of a gate dielectric layer disposed superjacent the bottom portion of the recess, adjacent the tapered sidewalls, and superjacent a portion of a top surface of the substrate, and a gate electrode completely overlying the gate dielectric layer. Gardner does not teach such a limitation, and therefore does not anticipate claim 4.

Gardner teaches a gate dielectric layer 128 formed in a channel region between two spacer structures (Col. 8, lines 42-44). Since the spacers 126 are formed in the trench region 106, if the gate dielectric layer 128 is formed *between* the two spacers 126, the gate dielectric layer is not formed over a top surface of the substrate. As a result, Gardener does not teach all the limitations of claim 4, and therefore does not anticipate claim 4.

Gardner also teaches a gate layer 130 that is level with a top surface of a substrate 100 (See Fig. 10). The conductive gate layer 130 is removed exterior to the trench (Col. 8, lines 61-64). Since there is no portion of the gate layer 130 that is outside of the trench, it cannot be said that Gardner teaches a gate electrode completely overlying a gate dielectric layer that is superjacent a portion of a top surface of a substrate, as in claim 4. As a result, Gardner does not anticipate claim 4.

Claims 5 and 6 depend from the independent claim 4, and therefore include all the limitations of claim 4. Since claim 4 is not anticipated by Gardner, claims 5 and 6 are also not anticipated by Gardner.

Examiner rejected claims 7-9 under 35 U.S.C. § 102(b) as being anticipated by U.S. Patent No. 5,342,796 (hereinafter "Ahn").

Claim 7 includes a limitation of a gate dielectric layer disposed superjacent the curvilinear recess and superjacent a portion of a top surface of the substrate. Ahn does not teach such a limitation. As a result, since Ahn does not teach all the limitations of claim 7, claim 7 is not anticipated by Ahn.

As can be seen in Figure 9, both the gate oxide film 7 and the spacers 12 are beneath a top surface of the substrate. After a polysilicon layer 8 is deposited, the polysilicon is removed everywhere except in the gate region G (Col. 4, lines 31-37, See Figure 7). The gate region G, as seen in Figure 7, encompasses the recessed portion of the substrate. Therefore, Ahn does not teach a gate dielectric layer disposed superjacent a portion of a top surface of the substrate, and Ahn does not anticipate claim 7.

Claims 8 and 9 depend from the independent claim 7, and therefore include all the limitations of claim 7. Since claim 7 is not anticipated by Ahn, claims 8 and 9 are also not anticipated by Ahn.

CONCLUSION

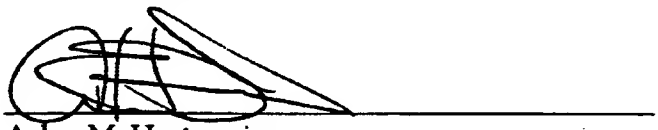
Applicants respectfully submit the present application is in condition for allowance. If the Examiner believes a telephone conference would expedite or assist in the allowance of the present application, the Examiner is invited to call Arlen M. Hartounian at (408) 720-8300.

Authorization is hereby given to charge our Deposit Account No. 02-2666 for any charges that may be due.

Respectfully submitted,

BLAKELY, SOKOLOFF, TAYLOR & ZAFMAN

Date: 4/23/04



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